Customer No.: 31561
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Application No.: 10/707,684

In The Claims:

Claim 1. (currently amended)A chip package structure, comprising:

a carrier;

a chip, having an active surface with a plurality of bumps thereon, wherein the chip is flipped over and bonded to the carrier in a flip-chip bonding process so that the chip and the carrier are electrically connected;

a heat sink, set over the chip, wherein the chip is separated from the heat sink by a distance between 0.03 ~ 0.2mm; and

an encapsulating material layer, filling a bonding gap between the chip and the carrier as well as a gap between the heat sink and the chip, wherein the encapsulating material layer is formed in a simultaneous molding process and part of the surface of the heat sink away from the chip is exposed.

Claim 2.(cancelled)

Claim 3. (original) The chip package structure of claim 1, wherein the encapsulating material layer has a thermal conductivity greater than 1.2W/m.K.

Claim 4. (original) The chip package structure of claim 1, wherein material constituting the encapsulating material layer comprises a resin.

Claim 5. (original) The chip package structure of claim 1, wherein material constituting the heat sink comprises a metal.

Claim 6. (original) The chip package structure of claim 1, wherein the package further

comprises an array of solder balls attached to a surface of the carrier away from the chip.

Claim 7. (original) The chip package structure of claim 1, wherein the package further comprises at least a passive component set on and electrically connected with the carrier.

Claim 8.(original) The chip package structure of claim 1, wherein the carrier is selected from a group consisting of a packaging substrate or a lead frame.

Claim 9. (currently amended) A chip package structure, comprising:

a carrier;

a chipset, set over and electrically connected to the carrier, wherein the chipset comprises a plurality of chips, at least one of the chips is bonded to the carrier or another chip in a flip-chip bonding process so that a flip-chip bonding gap is created;

a heat sink, set over the chipset, wherein the chipset is separated from the heat sink by a distance between 0.03 ~ 0.2mm; and

an encapsulating material layer, filling the flip-chip bonding gap and a gap between the chipset and the heat sink, wherein the encapsulating material layer is formed in a simultaneous molding process and part of the surface of the heat sink away from the chipset is exposed.

Claim 10. (cancelled)

Claim 11. (original) The chip package structure of claim 9, wherein the encapsulating material layer has a thermal conductivity greater than 1.2W/m.K.

Claim 12. (original) The chip package structure of claim 9, wherein the chipset at least comprises:

a first chip, having a first active surface, wherein the first chip is attached to the carrier such that the first active surface is positioned away from the carrier; and

a second chip, having a second active surface with a plurality of bumps thereon, wherein the second active surface of the second chip is bonded and electrically connected to the first chip in a flip-chip bonding process such that the bumps between the second chip and the first chip set a flip-chip bonding gap.

Claim 13. (original) The chip package structure of claim 12, wherein the chipset further comprises a plurality of conductive wires with ends connected electrically to the first chip and the carrier respectively.

Claim 14. (original) The chip package structure of claim 9, wherein the chipset at least comprises:

a first chip, having an active surface with a plurality of first bumps thereon, wherein the first active surface of the first chip is bonded and electrically connected to the carrier in a flip-chip bonding process such that the first bumps between the first chip and the carrier set a flip-chip bonding gap;

a second chip, having a second active surface, wherein the second chip is attached to the first chip such that the second active surface is positioned away from the first chip; and

a third chip, having a third active surface with a plurality of second bumps thereon, wherein the third active surface of the third chip is bonded and electrically connected to the second chip in a flip-chip bonding process such that the second bumps between the third chip and

the second chip set another flip-chip bonding gap.

Claim 15. (original) The chip package structure of claim 14, wherein the chipset further comprises a plurality of conductive wires with ends electrically connected to the second chip and the carrier respectively.

Claim 16. (original) The chip package structure of claim 9, wherein the material constituting the encapsulating material layer comprises a resin.

Claim 17. (original) The chip package structure of claim 9, wherein the material constituting the heat sink comprises a metal.

Claim 18. (original) The chip package structure of claim 9, wherein the package further comprises an array of solder balls attached to a surface of the carrier away from the chipset.

Claim 19. (original) The chip package structure of claim 9, wherein the package further comprises at least a passive component set on and electrically connected with the carrier.

Claim 20. (original) The chip package structure of claim 9, wherein the carrier is selected from a group consisting of a packaging substrate or a lead frame.